

VMFG-10G/20G-SMA

FEATURES

- ◆ Output Frequency: 10GHz~20GHz
- ◆ Frequency Step: 0.5MHz
- ◆ Dimension: 80mm×60mm×12mm
- ◆ Weight: ≤130g

TYPICAL APPLICATIONS

- ◆ X, Ku band Radar
- ◆ General Amplification

ELECTRICAL SPECIFICATIONS

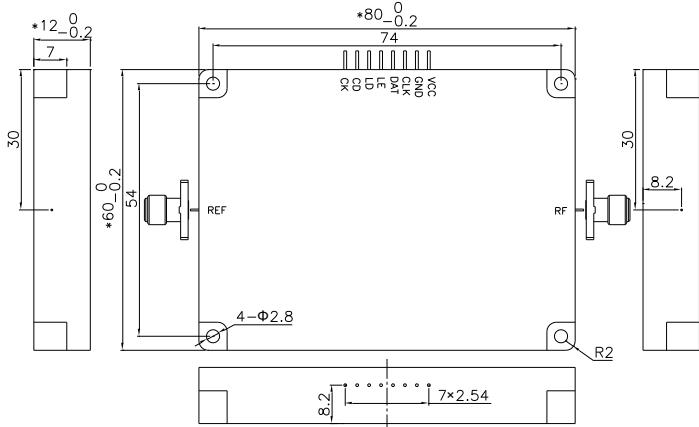
Input Clock Parameter	Min.	Typ.	Max.	Unit
Frequency	-	100	-	MHz
Level	6	-	10	dBm
Phase Noise	-	-	-130	dBc/Hz@100Hz
	-	-	-150	dBc/Hz@1kHz
	-	-	-165	dBc/Hz@10kHz
	-	-	-165	dBc/Hz@100kHz
	-	-	-73	dBc/Hz@100Hz
RF Output Parameter	Min.	Typ.	Max.	Unit
Frequency Range	10	-	20	GHz
Frequency Step	-	0.5	-	MHz
Frequency Setting time	-	-	200	μs
Output Power	-2	-	2	dBm
Phase Noise	-	-	-87	dBc/Hz@1kHz
	-	-	-96	dBc/Hz@10kHz
	-	-	-96	dBc/Hz@100kHz
	-	-	-106	dBc/Hz@1MHz
	-	-	-65	dBc
Spurious	-	-	-65	dBc
Lock Detect Level (Locked)	2.7	-	3.5	V
Lock Detect Level (Unlocked)	-	-	0.5	V
Other Parameter	Min.	Typ.	Max.	Unit
Vcc	5.5	6	6.5	V
Icc	-	-	1	A
Operation Temperature	-40	-	75	°C
Storage Temperature	-55	-	85	°C
Dimension	-	80×60×12	-	mm
Weight	-	-	130	g

OUTLINE AND INTERFACE

Unspecified tolerances: ± 0.2 mm. Only dimensions marked with * are inspected before shipment.

Housing material: Aluminum

Surface treatment: Natural conductive oxidation



Interface Definition			
No.	Symbol	Function	Note
1	REF	100M Clock Input	Φ0.38mm
2	RF	RF Output	Φ0.38mm
3	VCC	Power Supply	Φ0.6mm
4	GND	Ground	Φ0.6mm
5	CLK	SPI Clock	Φ0.6mm
6	DAT	SPI Data	Φ0.6mm
7	LE	SPI Enable	Φ0.6mm
8	LD	Lock Detect	Φ0.6mm
9	CD	Manufacturer reserved	Φ0.6mm
10	CK	Manufacturer reserved	Φ0.6mm

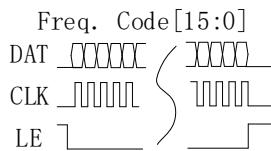
• CD, CK must be floating during operation.

• REF and RF interfaces utilize detachable SMA-K connectors. The unit is factory-equipped with SMA connectors by default.

APPLICATION NOTE

The module employs a 3-wire SPI synchronous serial interface (LE, DAT, CLK) with a maximum clock frequency of 10MHz. The control logic operates at 3.3V LVTTL levels.

Frequency Code Protocol:



The 16-bit frequency code is transmitted MSB-first. The host (waveform controller) must pull LE low for at least 1 clock cycle before initiating data transfer. Data (DAT) is output by the controller on CLK falling edges and sampled by the frequency synthesizer on CLK rising edges. After transmitting all 16 bits, LE is pulled high to latch the frequency setting.

Decimal frequency code range 0–20,000 corresponds to 10 GHz–20 GHz with a 0.5 MHz step size. Codes must be converted to hexadecimal before transmission (e.g., 19994.5 MHz = 0x4E15).

Default output frequency at power-up is 10 GHz. If an invalid code (outside 0–20,000) is received, the output retains the current frequency.

ABSOLUTE MAXIMUM RATINGS

Parameter	Function
VCC	7V
Input Power	14dBm
Pin soldering duration (300°C)	10s

SOLDERING & HANDLING INSTRUCTIONS

ESD-sensitive device – Avoid direct contact with I/O terminals to prevent electrostatic discharge (ESD) damage.

Handle with care during transportation/assembly – Avoid mechanical shock or drops to maintain circuit integrity.