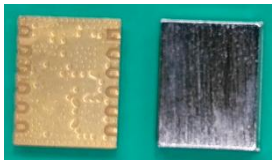
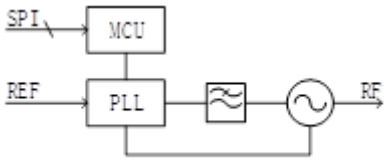
VMFG-3G/6G-SM1512

FEATURES



- Output Frequency：3000MHz~6000MHz
- Frequency Step：10MHz
- Integrated MCU, PLL, and VCO
- Dimension：15.0mm×12.0mm×2.5mm
- Weight：≤3g



TYPICAL APPLICATIONS

- S, C, X band Radar
- Military Radio
- General Amplification

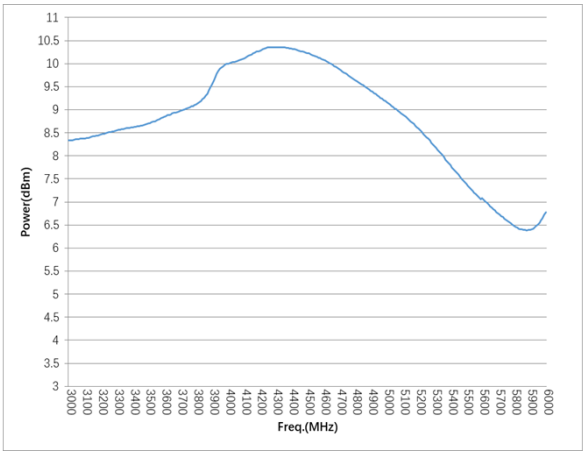
ELECTRICAL SPECIFICATIONS

(TA=25℃，VCC=3.3V，Input Frequency：100MHz，Input Power：0~5dBm，Input Phase Noise：-155dBc/Hz@1kHz)

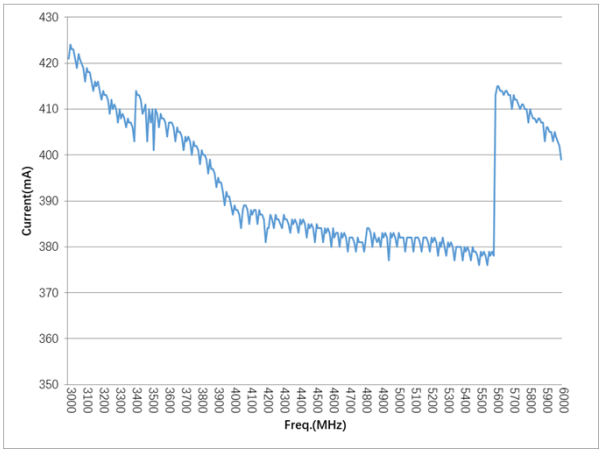
Parameter	Min.	Typ.	Max.	Unit
Output Frequency	3000	-	6000	MHz
Frequency Step	-	10	-	MHz
Frequency Setting time	-	-	40	μs
Phase Noise	-	-	-87	dBc/Hz@100Hz
	-	-	-99	dBc/Hz@1kHz
	-	-	-106	dBc/Hz@10kHz
	-	-	-105	dBc/Hz@100kHz
	-	-	-123	dBc/Hz@1MHz
	-	-	-140	dBc/Hz@10MHz
Output Power	5	-	-	dBm
Harmonic	-	-	-10	dBc
Spurious	-	-	-70	dBc
Lock Detect Level (Locked)	2.7	3.3	3.5	V
Lock Detect Level (Unlocked)	-	-	0.2	V
Current	-	-	450	mA

TYPICAL PERFORMANCE CHARACTERISTICS

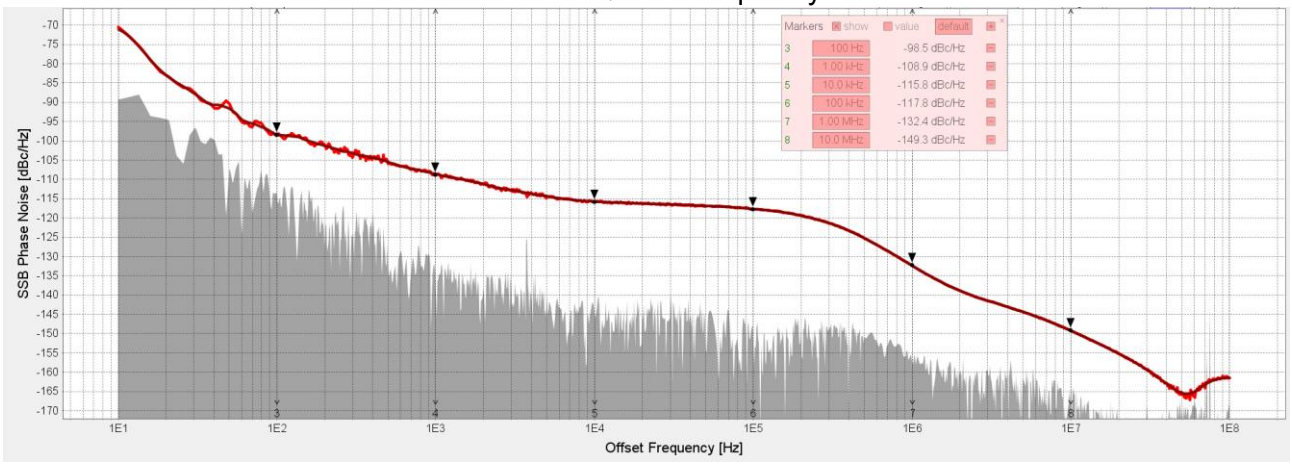
RF Ouput Power Vs Frequency（25℃）



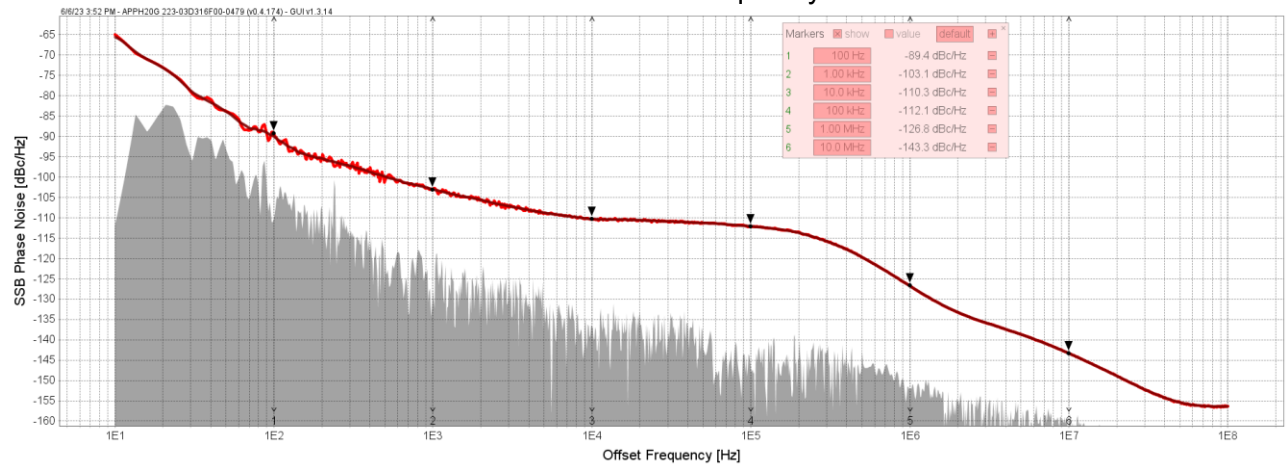
Current Vs Frequency（25℃）



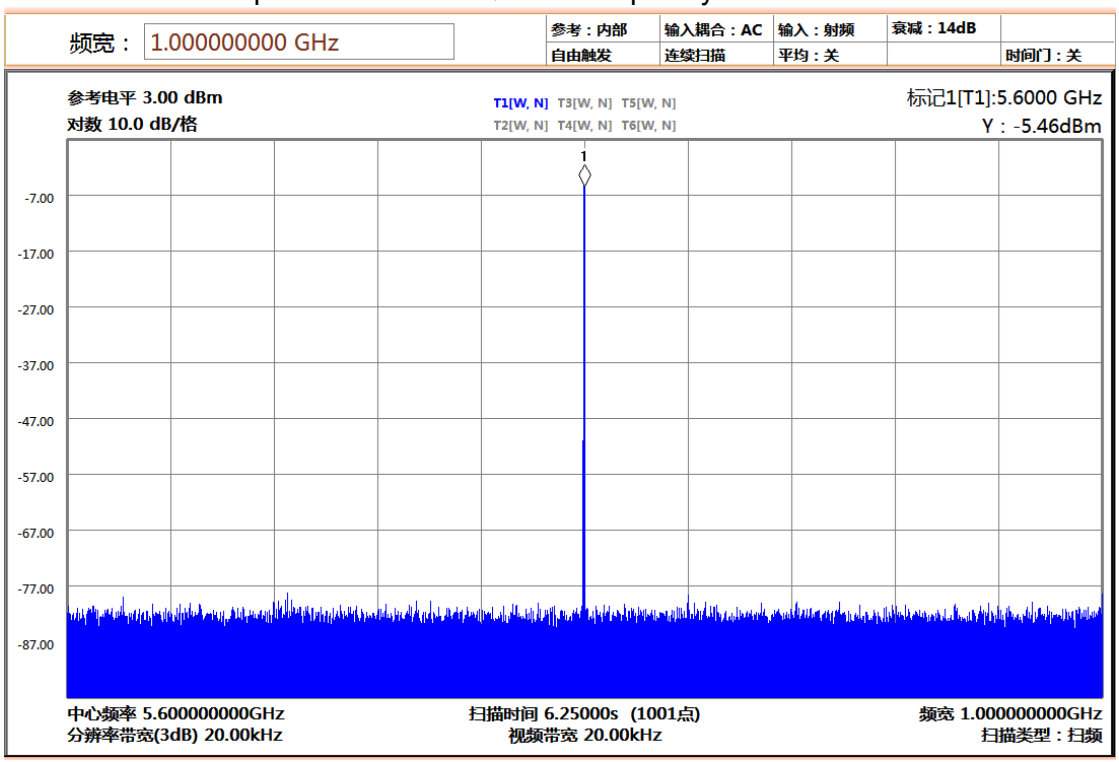
Phase Noise（TA=25℃，RF Frequency: 3000MHz）



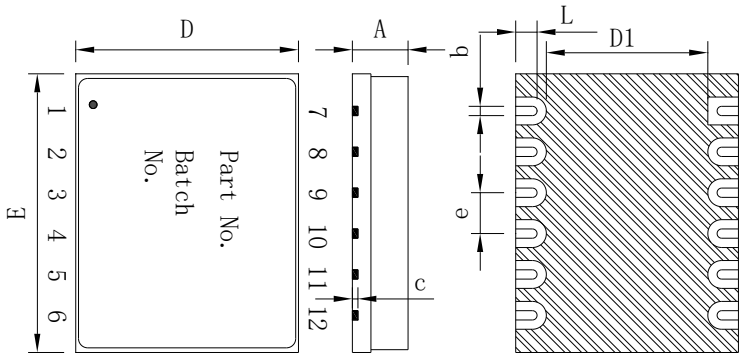
Phase Noise（TA=25℃，RF Frequency: 6000MHz）



Spurious（TA=25℃， RF Frequency: 5600MHz）



OUTLINE DRAWING



Symbol	Dimension(mm)		
	Min	Typ	Max
A	-	2.5	2.7
b	-	0.5	-
c	-	0.3	-
D	11.8	12.0	12.2
D1	-	8.7	-
e	-	2.2	-
E	14.8	15.0	15.2
L	-	1.15	-

Shielding enclosure material is nickel-plated stainless steel, The solder pads are gold-plated on the surface.

PIN FUNCTION

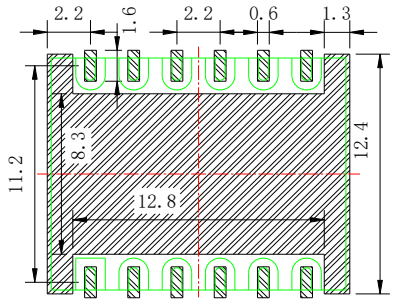
Pin No.	Function	Symbol	Pin No.	Function	Function
1	Clock In	REF	7	VCC	VCC
2	Manufacturer reserved	PC	8	Lock Detect	LD
3	Manufacturer reserved	PD	9	SPI enable	LE
4	NC	NC	10	SPI data	DAT
5	NC	NC	11	SPI clock	CLK
6	NC	NC	12	RF output	RF

Note 1：Pin No. 9~11 are 3.3V-LVTTL level。

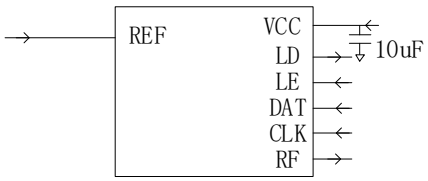
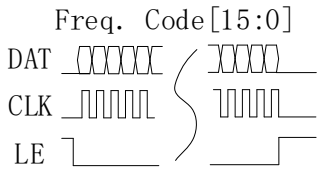
Note 2：Pin No.2~6 must remain unconnected (floating).

RECOMMENDED FOOTPRINT

Please use grounding vias on the bottom-side grounding pad in accordance with PCB fabrication rules to ensure proper product grounding.



APPLICATION NOTE

	For power supply, a low-noise LDO is recommended for secondary voltage regulation to minimize the introduction of power supply noise and interference. A 10μF decoupling capacitor should be placed in close proximity to the power input for effective noise filtering. The frequency-hopping control utilizes a 3-wire SPI synchronous serial interface (LE, DAT, CLK), with a maximum serial clock frequency of 10 MHz.
	The frequency code consists of 2 bytes. During transmission, the most significant byte (MSB) is sent first. After pulling LE (Latch Enable) low for at least 0.1 μs, the host transmits DAT (Data) on the falling edge of CLK (Clock), while the device samples DAT on the rising edge of CLK. After sending all 16 bits, LE is pulled high. The frequency code's decimal range of 0–300 corresponds to an output frequency range of 3000 MHz–6000 MHz. During transmission, the decimal value must be converted to hexadecimal. For example: To set an output frequency of 5880 MHz, transmit 01 20. If the input frequency code is outside the valid range (0–300), the output frequency remains unchanged.

ABSOLUTE MAXIMUN RATINGS

Parameter	Function
VCC	+3.5V
Input power	+13dBm
Reflow Soldering Peak Temperature	255℃/30Sec